

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): TSURUTA	Atty. Dkt.: 11-202
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: SEMICONDUCTOR SUBSTRATE AND MANUFACTURING PROCESS THEREFOR	

Commissioner for Patents
Arlington, VA 22202

Date: November 4, 2003

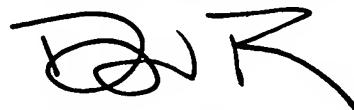
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are being submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



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Form PTO-1449		ATTORNEY DOCKET NO.	SERIAL NO.
<p>PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p> <p>Sheet 1 of 1</p>		11-202	
		APPLICANT	
		Kazuhiro TSURUTA	
FILING DATE	GROUP		
11/4/03			

U.S.PATENT DOCUMENTS						
Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
		4,139,442	2/13/79	Bondur et al.		
		4,238,278	12/9/80	Antipov (corres. to JP 58-37988)		
		4,910,165	3/20/90	Lee et al.		
		5,548,150	8/20/96	Omura et al.		
		5,736,749	4/7/98	Xie		
		6,504,227	1/7/03	Matsuo et al. (corres. to JP 2001-77315)		
FOREIGN PATENT DOCUMENTS						
Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation
		55-78540	6/13/80	Japan		<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
		58-37988	8/19/83	Hirobe		<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No
		2001-77315 <i>(Discussed in pages 2-3 in the spec.)</i>	3/23/01	Japan		<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No
		2001-527292	12/25/01	Matsuo et al.		<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No
				Japan		<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No
				Erzgraber		<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
		"REDUCING SILICON-SUBSTRATE PARASITICS OF ON-CHIP TRANSFORMERS" by Jiang et al.; Technical Digest of The 15th IEEE International Conference on Micro Electro Mechanical Systems; 2002; pp., 649-652 (<i>Discussed in page 4 of the spec.</i>)
		"FABRICATION OF THICK SILICON DIOXIDE LAYERS USING DRIE, OXIDATION AND TRENCH REFILL" by Zhang et al.; Technical Digest of The Fifteenth IEEE International Conference on Micro Electro Mechanical Systems; 2002; pp., 160-163 (<i>Discussed in pg 3-4 in the spec.</i>)
		"Large Suspended Inductors on Silicon and Their Use in a 2- m CMOS RF Amplifier" by Chang et al.; IEEE Electron Device Letters, Vol. 14, No. 5; 1993; pp., 246-248 (<i>Discussed in pg 2 of the spec.</i>)
		"A Novel Buried Oxide Isolation for Monolithic RF Inductors on Silicon" by Erzgraber et al.; IEDM98-535 (1998); pp., 1-5

EXAMINER:	Date Considered:
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EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.